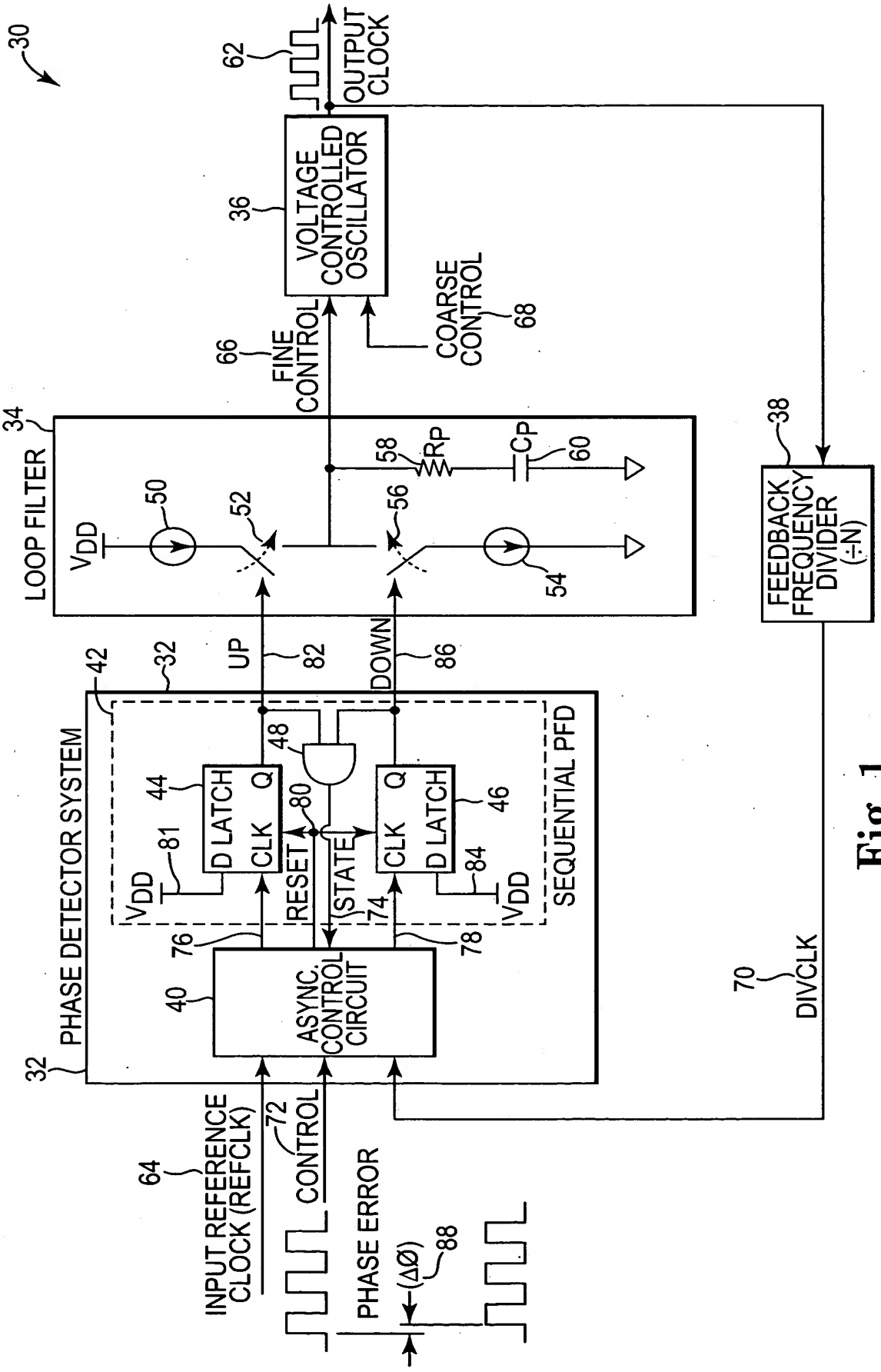
30
62
OUTPUT CLOCK
36
VOLTAGE CONTROLLED OSCILLATOR
COARSE CONTROL
68
66
FINE CONTROL
34
LOOP FILTER
VDD
50
52
56
58
RP
CP
60
54
38
FEEDBACK FREQUENCY DIVIDER (÷N)
42
32
UP
82
DOWN
86
PHASE DETECTOR SYSTEM
SEQUENTIAL PFD
48
44
D LATCH
CLK
Q
80
81
RESET
STATE
74
46
84
76
78
40
ASYNC. CONTROL CIRCUIT
70
DIVCLK
64
INPUT REFERENCE CLOCK (REFCLK)
72
CONTROL
PHASE ERROR
(ΔØ)
88

Fig. 1

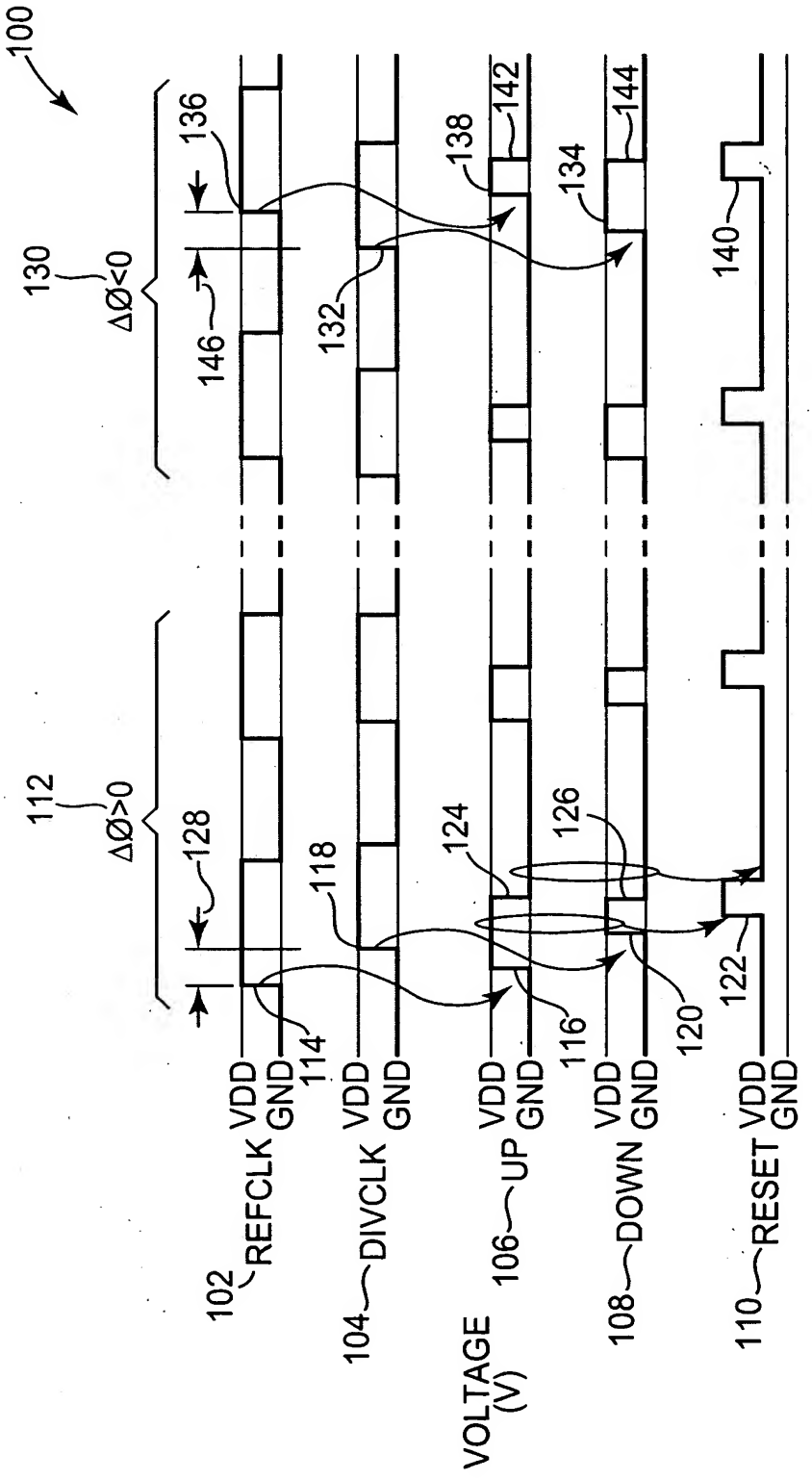
100
130
ΔØ<0
112
ΔØ>0
136
146
128
132
138
142
134
144
140
118
124
126
114
116
120
122
VDD
GND
REFCLK
DIVCLK
UP
DOWN
RESET
102
104
106
108
110
VOLTAGE (V)
TIME(t)

Fig. 2

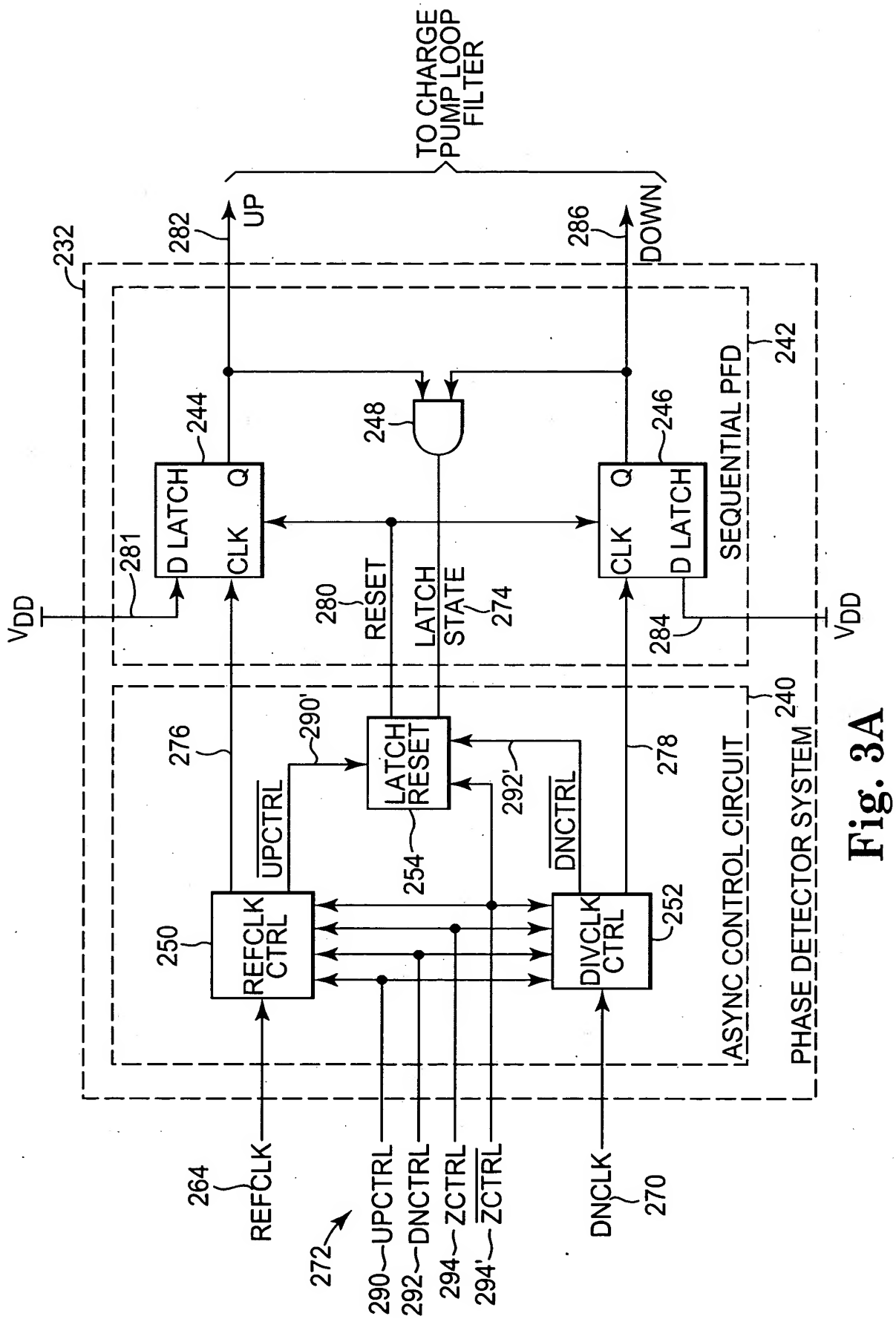
TO CHARGE PUMP LOOP FILTER
UP
DOWN
282
286
232
242
SEQUENTIAL PFD
244
246
248
D LATCH
Q
CLK
281
280
RESET
LATCH STATE
274
284
VDD
240
PHASE DETECTOR SYSTEM
ASYNC CONTROL CIRCUIT
276
290'
278
LATCH RESET
UPCTRL
DNCTRL
292'
254
250
252
REFCLK CTRL
DIVCLK CTRL
264
REFCLK
272
UPCTRL
DNCTRL
ZCTRL
ZCTRL
290
292
294
294'
DNCLK
270

Fig. 3A

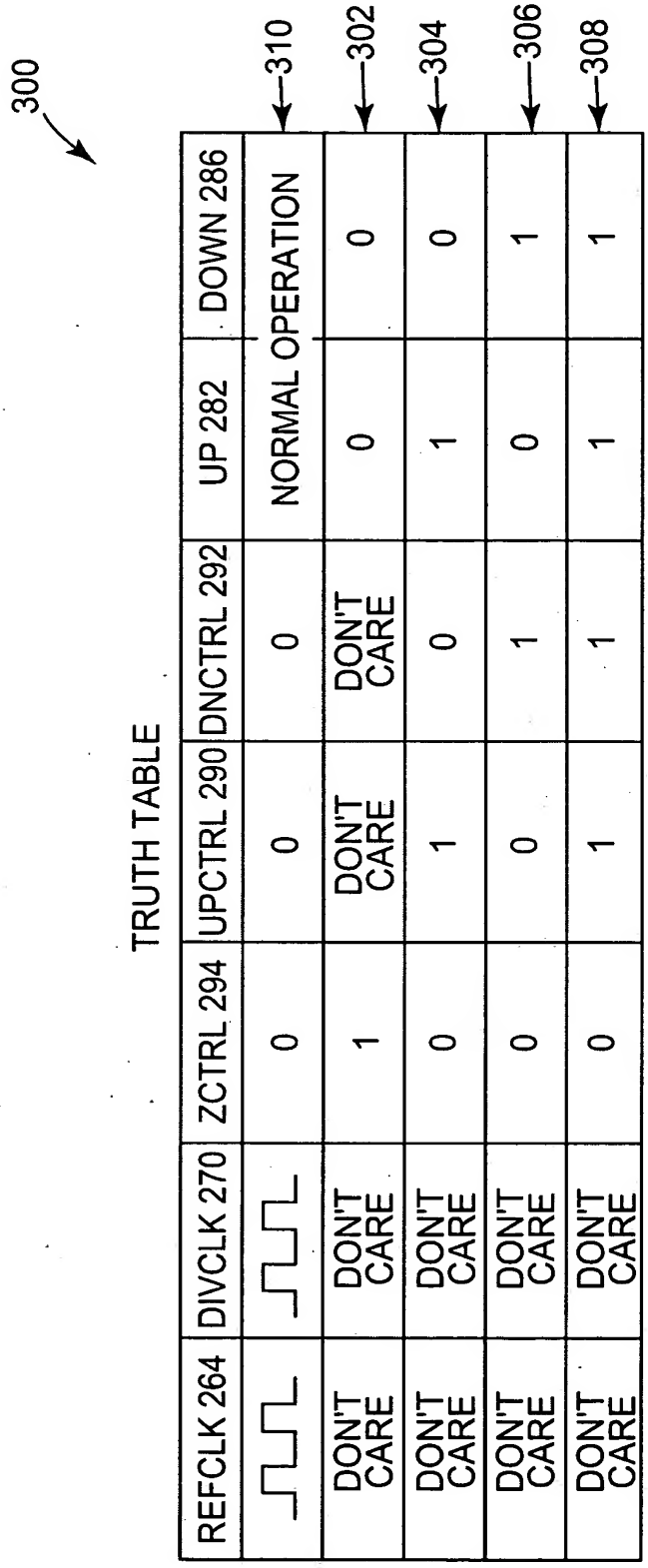
300
TRUTH TABLE
REFCLK 264
DIVCLK 270
ZCTRL 294
UPCTRL 290
DNCTRL 292
UP 282
DOWN 286
NORMAL OPERATION
DON'T CARE
0
1
310
302
304
306
308

Fig. 3B

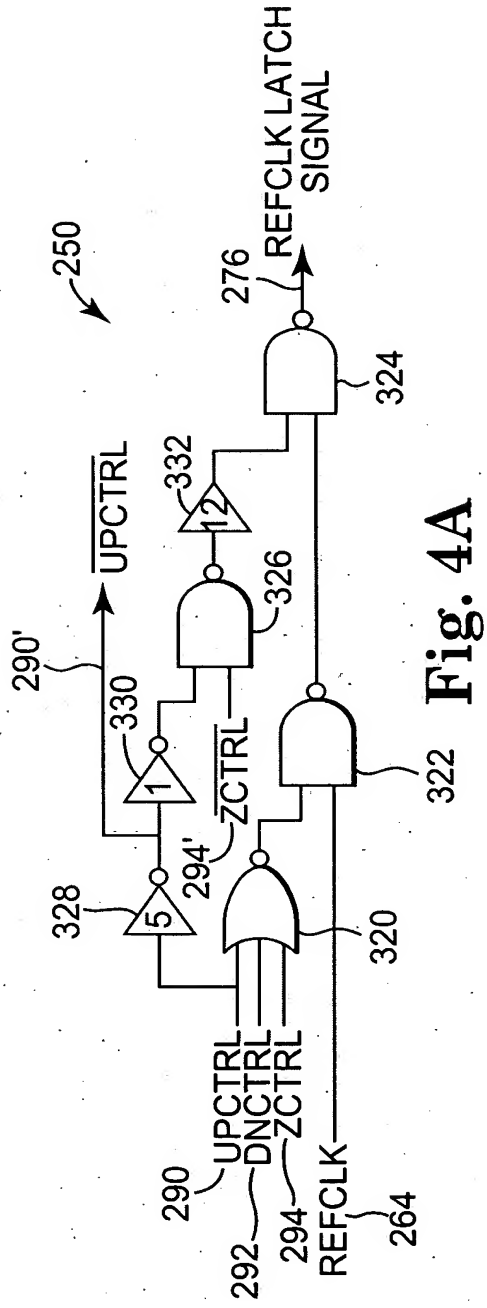
250
276
REFCLK LATCH SIGNAL
324
332
12
326
UPCTRL
290'
330
1
ZCTRL
294'
328
5
322
320
UPCTRL
DNCTRL
ZCTRL
290
292
294
REFCLK
264

Fig. 4A

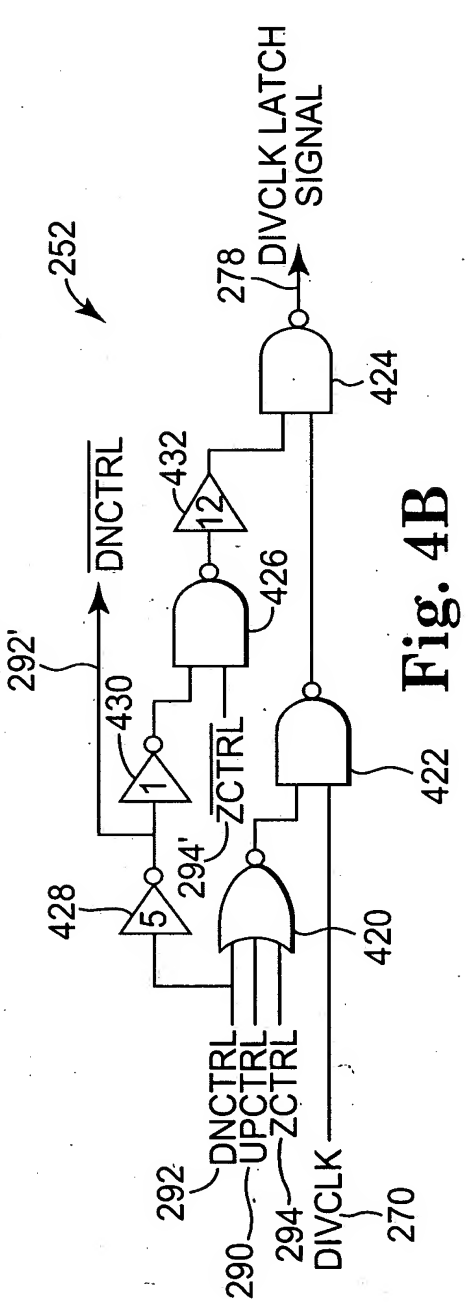
252
278
DIVCLK LATCH SIGNAL
424
432
12
426
DNCTRL
292'
430
1
ZCTRL
294'
428
5
422
420
DNCTRL
UPCTRL
ZCTRL
292
290
294
DIVCLK
270

Fig. 4B

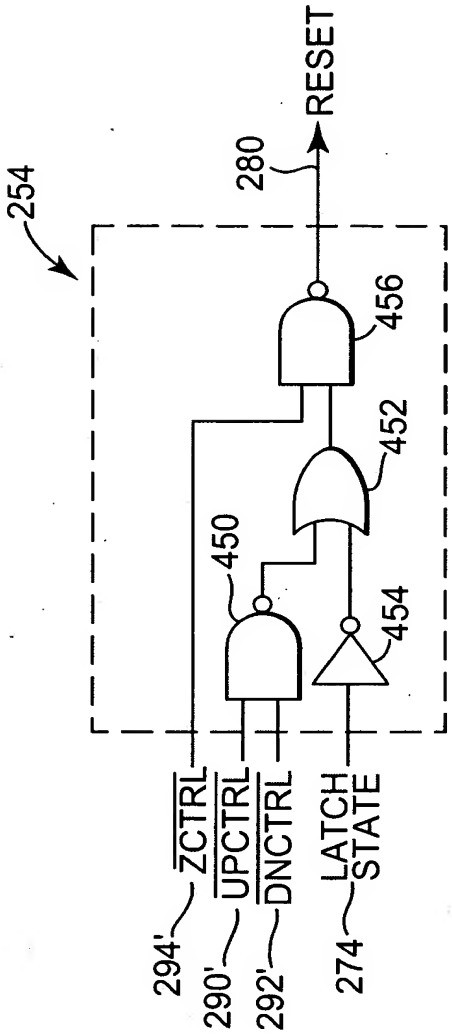
254
280
RESET
456
452
450
454
294'
ZCTRL
290'
UPCTRL
292'
DNCTRL
274
LATCH STATE

Fig. 4C